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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,515	12/17/2003	Shinji Nishimura	NITT-169	6112

38327 7590 02/06/2007

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EXAMINER	
PANWALKAR, VINEETA S	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/736,515	NISHIMURA ET AL.	
	Examiner	Art Unit	
	Vineeta S. Panwalkar	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7,11,12 and 16-20* is/are allowed.

6)☒ Claim(s) *8-10 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1a. Claim 14 recites the limitation "the variable gain amplifiers" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Raghavan et al. (US 2003/0102911 A1), hereinafter, Raghavan.

2a. Regarding claim 8, Raghavan shows a phase shifting method of shifting a phase of an input signal (Fig. 2, Linearizer 18 is interpreted as performing claimed phase shifting), comprising the steps of:

- dividing the input signal into a first signal and a second signal (Fig. 2, Splitter 20 divides input signal into I and Q signals (claimed first and second signals));
- giving a phase difference between the first signal and the second signal (Fig. 2, Splitter 20 gives a 90 degree phase shift to the Q signal, thereby giving a phase difference between I and Q signals); and
- when adding the first signal to the second signal to attain an output signal, controlling the amplitudes of the first signal and the second signal to thereby shift a phase of the output signal (Fig.2, Summer26 adds the I and Q signals and RF OUT is interpreted as claimed output signal. Variable gain amplifiers 22 and 24 perform the claimed controlling of amplitudes of the I and Q signals. Since increasing the gain in one amplifier while reducing the gain in the other, alters the phase with constant amplitude, it is interpreted as interpreted as claimed phase shifting of output signal).

(See Fig. 2 and paragraphs [0018] –[0020]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject

matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan in view of Iinuma et al. (US 5175514), hereinafter, Iinuma.

3a. Regarding claim 9, Raghavan shows all the limitations claimed (see 2a above), but fails to show details of the type of signals used.

In the same field of endeavor, however, Iinuma shows a circuit (Fig. 1) wherein : using a low-frequency factor of a clock signal or a data signal as the input signal, forming a rectangular wave signal from the output signal, and thereby shifting a phase of the clock signal or the data signal. (Fig. 1, a mapping circuit 2 outputs I phase and Q phase components of a modulating wave signal as rectangular signals (Thus output of the summer 9 would also be rectangular signal) in response to a digital baseband signal (claimed low frequency input) applied through an input terminal 1.Elements 5, 6, 7 and 8 perform claimed phase shifting. See column 1, lines 57-64).

Thus, it would have been obvious to a person of ordinary skill in the art that for a low frequency input, the phase shifting would provide a rectangular output because it results in efficient transmission (Column 1, lines 15-20).

4. Claims 10, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US 6079035, hereinafter, Suzuki), in view of Goldrain (US 5742798).

4a. Regarding claim 10, Suzuki discloses a skew compensation system (the computer system shown in Fig.1 is interpreted as claimed skew compensation system wherein circuit 30 (Fig. 3) performs the skew compensation) used for high-speed parallel signaling, wherein the skew compensation system shifts phase differences between a high-speed synchronized clock signal and parallel data signals, the skew compensation system comprising: a circuit located on a receiver side for controlling phase differences between the clock signal and the data signals;

(See Figs 1, 2 and 3. The receiver circuit 24 of Fig. 2 comprises a parallel data skew detecting circuit 30 as shown in FIG. 3. The parallel data skew detecting circuit 30 includes a plurality of data channels CH1-CH12 (claimed parallel data signals. Since the data rate is 1 GHz, the system is interpreted to be transmitting high-speed parallel data, as claimed) in which corresponding data signals DIN01-DIN11 are transported from the lines in the fiber-optic ribbon 13. A shift register

set 31 is connected to the first data channel CH1. The shift register set 31 comprises a plurality of serial shift registers 31a14 31e. Each of the shift registers 31a-31e sequentially outputs received data signal DIN0 in synchronization with a sampling clock CLK (claimed synchronized clock) supplied from a sampling clock generating circuit, not shown. Thus, the shift registers are interpreted as performing claimed shifting. See column 3, line 47 – column 4, line 17).

wherein a special data pattern defined to be used is transmitted when a synchronized data transmission cannot be realized because of a skew between parallel data lines being not yet adjusted on the receiver side or before transmitting the data signals every constant time cycle from a transmitter side; and wherein the circuit receives signals outputted from a transmitter side circuit to detect errors of the signals to the defined special data pattern, and shifts the phase differences between the clock signal and the data signals on basis of a result of the detection at the receiver side so that the special data pattern is received correctly at the receiver side, and a system installed in the circuit, and

(Suzuki's parallel data skew detecting circuit includes: a plurality of parallel data channels including a plurality of serial shift registers for passing a sample signal (claimed special data pattern), a timing signal generating circuit generated a timing signal in a predetermined period and a skew storage circuit to record the shift register which receives the sample signal for the respective data channels when the timing signal is generated. The shift register which receives the sample signal at the time of generating the timing signal can be identified among the shift

registers sequentially transporting the received sample signal in each of the data channels. The sample signals output from the identified shift registers are simultaneously output from all of the data channels. Skew can accordingly be detected in the parallel transmission data. The parallel data skew detecting circuit further includes a gate circuit capable of allowing a coming data signal to output from the shift register recorded in the skew storage circuit in the data channel. Once the shift registers are recorded in all of the data channels based on the sample signal, subsequent data signals are guided through the recorded shift registers so as to synchronize with one another. Skew can accordingly be compensated in the parallel transmission data in this way. Thus, the sample signal (claimed special data pattern) is used to detect the skew (claimed error) and based on this detection, the correction needed to synchronize the sample signal is recorded and used for all subsequent data. (See column 1, line 29 – column 2, line 30). The sample data is sent when the signal for indicating the beginning of the skew detecting operation is received. This may include a power-on-reset which is generated when the system is turned on. The power-on-reset is transmitted from the host computer 12 to the input/output unit 11 over a line for power supply control, not shown, which line is independent from the passage of the data transmission. A reset signal is supplied to the parallel data skew detecting circuit 30 in response to the signal in the optical transmitter/receiver module 15 for the input/output unit 11. These reset signals serve to reset all of the logic gate circuits 35a-35e. When the timing signal generating circuit 37

receives the reset signal Enable, it starts to operate. Thus, the sample signal is sent when before transmitting data, as claimed. Although Suzuki does not explicitly mention the use of sample signal every constant data cycle, it would have been obvious to a person of ordinary skill in the art to use such a signal every so often, to ensure proper synchronization. Further, the skew compensation is achieved by shifting the phase of either of the clock signal or the parallel data signals, so that synchronization is achieved. Column 4, lines 27-58). Thus, Suzuki discloses all the limitations claimed, but fails to disclose how the exact details of how the exact shifting of phase is achieved.

In the same field of endeavor, however, Goldrain shows skew compensation circuitry wherein,

the system shifts the phase of either of the clock signal or the parallel data signals by dividing the phase for one cycle of the base frequency of the synchronized clock signal into time cycles of x units (x: integer not less than 2) with even time cycle or uneven time cycle to compensate the skew.

(FIG. 9D shows the situation where clock A is delayed by one quarter of a clock cycle (930) (This is interpreted as dividing the phase for one cycle of base frequency of the clock by x units (in this case 4, which is an integer greater than 2)). Clock A (930) and clock B (933) are in phase, the clock skew is compensated, as claimed.)(Column 8, lines 15-51).

Thus, it would have been obvious to a person of ordinary skill in the art to use Goldrain's skew compensation method because a very accurate elimination of clock skew can be achieved. (Column 2, lines 23-25).

4b. Regarding claim 13, Suzuki and Goldrain show all the limitations claimed (See 4a above).

Goldrain further shows the how the adjustment of the variable clock delay on chip allows to synchronize chip clock A and B with respect to each other (Thus, the of variable delay adjustment to perform phase shifting for synchronization (as claimed) is disclosed).

4c. Regarding claim 15, Suzuki and Goldrain show all the limitations claimed (See 4a above).

Although neither Suzuki nor Goldrain disclose the claimed type of special data, since 8B10B and 64B66B codes in Ethernet standard are known, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use characters recognized in the standard as the claimed special data pattern in order to be compatible with the Ethernet standard.[1]

[1] References showing 8B10B/64B66B codes in Ethernet standard:
- Nishi (US 2003/0223587 A1)
- Collins (US 2003/0046618 A1)
- Herrity (US 2002/0131105 A1)

Allowable Subject Matter

5. Claims 1-7, 11,12, and 16-20 are allowed.

The following is an examiner's statement of reasons for allowance:

5a. Regarding claim 1, prior art of record fails to show a phase shifter comprising first filter, first and second signal paths, phase shift element, first and second variable gain amplifiers, adder-subtractor and second filter, exactly as claimed. The claim has been interpreted in light of specification, especially Fig. 11 and page 21, line 5- page 22, line 3.

5b. Claims 2-7 are allowed as being dependent on claim 1.

5c. Regarding claim 11, prior art of record fails to show a skew compensation system used for high-speed parallel signaling, wherein the skew compensation system shifts phase differences between a high-speed synchronized clock signal and parallel data signals, the skew compensation system comprising a circuit that the phase shifting circuit has, wherein the circuit, in order to shifts the phase of either of the clock signal or the parallel data signals by dividing the phase for one cycle of the base frequency of the synchronized clock signal into time cycles of x units (x: integer not less than 2) with even time cycle or uneven time cycle to compensate the skew, executes a filtering processing to one of the clock signal or the data signals through a band pass filter having a pass band not higher than the base frequency of the synchronized clock signal, divides the filtered signal into plural signals of more than or equal to two, inputs the signals after being divided to phase shifter elements each having different propagation delay

characteristics, inputs signals from the phase shifter elements to different variable gain amplifiers respectively, after adding outputs from the variable gain amplifiers, inputs a signal after being added to a limit amplifier having a pass band characteristic sufficiently higher than the based frequency of the synchronized clock signal to reshape the waveform of the signal after being added into a rectangular wave, and inputs a signal after being reshaped to a flip-flop circuit together with the parallel data signals or the clock signal paired with the reshaped signal to execute a re-timing processing, and wherein the phase shifting circuit, by individually adjusting the outputs from the plural variable gain amplifiers incorporated in the circuit, shifts the phases of the output signals from the limit amplifier of the data signals or the clock signal to be phase-shifted to x levels with the signal factors retained intact, and realizes shifting the phase differences between the clock signal and the data signals by using the above phase-shifting function, in combination with each and every other limitation of the claim. Claim is interpreted in light of the specification.

5d. Claims 16 and 19 are allowed as being dependent on claim 11.

5e. Regarding claim 12, prior art of record fails to show a skew compensation system used for high-speed parallel signaling, wherein the skew compensation system shifts phase differences between a high-speed synchronized clock signal and parallel data signals, the skew compensation system wherein claimed wherein first circuit receives signals outputted from a transmitter side circuit to detect errors of the signals to the defined special data pattern, and adjusts the phase

differences between the clock signal and the data signals on basis of a result of the detection at the receiver side of the data so that a phase relation for receiving the special data pattern correctly at the receiver side is obtained, and a second circuit that the first circuit has, wherein the second circuit, in order to shifts the phase of either of the clock signal or the data signals by dividing the phase for one cycle of the base frequency of the synchronized clock signal into-time cycles of x units (x: integer not less than 2) with even time cycle or uneven time cycle, executes a filtering processing to one of the clock signal or the data signals through a band pass filter having a pass band not higher than the base frequency of the synchronized clock signal, divides the filtered signal into plural signals of more than or equal to two, inputs the signals after being divided to phase shifter elements each having different propagation delay characteristics, inputs signals from the phase shifter elements to different variable gain amplifiers respectively, after adding or subtracting outputs from the variable gain amplifiers by means of an adder-subtracter, inputs a signal after being added or subtracted to a limit amplifier to a limit amplifier having a pass band characteristic sufficiently higher than the based frequency of the synchronized clock signal to reshape the waveform of the signal after being added or subtracted into a rectangular wave, and inputs a signal after being reshaped to a flip-flop circuit together with the data signals or the clock signal paired with the reshaped signal to execute a re-timing processing, and wherein the first circuit, by individually adjusting the outputs from the plural variable gain amplifiers incorporated in the second circuit

and using to switch the adding and subtracting functions, shifts the phases of the output signals from the limit amplifier of the data signals or the clock signal to be phase-shifted to x levels with the signal factors retained intact, and realizes shifting the phase differences between the clock signal and the data signals by using the above phase-shifting function,, in combination with each and every other limitation of the claim. Claim is interpreted in light of the specification.

5f. Claims 17, 18 and 20 are allowed as being dependent on claim 12.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Feher (US 6757334 B1) shows in-phase and quadrature phase signals followed by amplifiers.
- Lee et al (US 5719862) show dynamic de-skewing wherein a unique flag is used to determine the amount of skew compensation required.

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VP.